REMARKS

Reconsideration and allowance of this application are respectfully requested. Claims 1 and 2 are currently amended. Claims 3-20 were previously cancelled. New claims 21-33 are added. Accordingly, claims 1-2 and 21-33 are submitted for the Examiner's consideration.

In the Office Action, the Examiner rejected claims 1-2 under 35 U.S.C. § 103(a) as being unpatentable over Kenney (U.S. Patent No. 6,020,250) in view of Cogan (U.S. Patent No. 4,845,051) and further in view of Kagaya (U.S. Patent No. 5,523,593). It is submitted, however, that the claims are patentably distinguishable over the references.

The Kenney patent is concerned with sub-surface *contact structures* to stacked semiconductor devices. Kenney shows, in Figs. 5c - 5d, a single vertical trench 172 that provides both *input and output contacts to a CMOS invertor*. A narrower, lower part of the trench includes sidewall insulators 176 and a conductive layer 208a that fills the bottom portion of the narrower part of the trench and contacts doped region 180' at the bottom of the trench. A thin insulator layer 210 covers the top of the conductive layer 208a as well as the exposed portions of the sidewall insulators 176. The remainder of the narrower part of the trench as well as an upper, wider part of the trench are filled with a second conductive layer 214. (See col. 13, lines 51-55; and col. 14, line 47 to col. 15, line 12). Kenney also describes other vertical trench structures as *source and drain contacts* to FETs as well as *contacts* to bipolar transistors. There is no suggestion in the reference of using any of these structures for an *isolation trench*.

Moreover, the Examiner's proposed use of Kenney's vertical trench 172 as an isolation trench changes the principle of operation of Kenney's vertical trenches. Instead of using

Kenney's vertical trench as a contact, wherein current passes through the conductive layer within the trench, the Examiner proposes using the vertical trench to provide electrical isolation from other semiconductor devices wherein, as a person of ordinary skill in the relevant art would understand, the conductive layer of the vertical trench is *not* intended to conduct current. Clearly, the Examiner's proposed use of Kenney's vertical trench changes the basic principle under which the trench structure is designed to operate and cannot be used to render the claims obvious. MPEP § 2143.01.

As acknowledged by the Examiner, Kenney does not suggest filling an upper portion of the trench with an electrical insulator or suggest a trench enclosing an area of the semiconductor body. The Examiner therefore relies on the Cogan patent to teach filling the upper portion of the trench with an electrical insulator. Cogan describes a trench structure that provides a buried gate for an n-channel JFET. The lower part of the trench is filled with P+ polysilicon which serves as a gate electrode to a P-type gate region 23 that is located beneath the trench as well as along the sides of the lower part of the trench. A low temperature oxide (LTO) 24 fills the upper part of the trench. The LTO layer 24 and an upper part of the P+ polysilicon 22 are isolated from the N-substrate 12 by silicon oxide sidewalls 20. (See Figs. 2j and 3-5; and col. 5, lines 24-62).

Cogan, however, describes that window regions 26a must be etched into the LTO layer 24 to form contact holes in the LTO layer to the gate polysilicon region 22 which are then filled with a metal layer to form a gate contact 28a. (See Figs. 2i and 2j; and col. 5, lines 6-41). Because Cogan requires that contact holes filled with a metal layer are formed within the

LTO layer, the reference cannot suggest that a remaining portion of the isolation trench is *filled* with an electrical insulator.

Further, though Cogan shows, in Figs. 2g and 2h, the LTO layer without such contact holes, the JFET cannot operate unless the contact holes 26a are formed and filled with the gate contact metal because Cogan does not describe any other contact to the polysilicon gate 22. Therefore, Cogan *teaches away* from not incorporating the openings into the LTO layer and thereby *teaches away* from a *remaining portion* of a trench *being filled* with an electrical insulator.

The Examiner's proposed modification of the LTO layer of Cogan to fill the remaining portion of the trench without contact holes or a metal contact thus renders Cogan's JFET device inoperable and unsatisfactory for its intended purpose. Therefore, the Examiner cannot properly rely on Cogan providing suggestion or motivation to modify the LTO layer in this manner. MPEP § 2142.01.

Though the Examiner acknowledges that neither Kenney nor Cogan discloses a trench enclosing an area of the semiconductor body, the Examiner contends that Kagaya does. Kagaya shows, in Fig. 1, etched trenches 9 which enclose the periphery of a FET. The patent also shows, in Fig. 26, filling an entire trench 232 with an insulator 241. Kagaya, however, does not suggest modifying Kenney's trench that provides *electrical contacts* to a *CMOS invertor, FET or bipolar transistor* or suggest modifying Cogan's trench that provides *electrical contacts* to the *buried gate of a JFET* to form an *isolation trench* in the manner called for in the claims.

It follows that the Examiner has improperly combined the Kenney, Cogan and Kagaya references by putting together "bits and pieces" of the structures of three very different devices in a manner that none of the references suggest.

Specifically, the Examiner has combined part of a trench that provides input and output contacts to a CMOS invertor, FET or bipolar transistor (of Kenney) with a piece of a buried gate trench of an n-channel JFET (of Cogan) and then extends the combined pieces of the two devices around an area of another device as described in Kagaya with respect to a trench filled with an insulator. The only way that the Examiner could have taken the pieces the three structures and combined them in this manner is by using hindsight derived from the teachings of the present application. There is no suggestion in any of the references to carry out these modifications.

Absent a suggestion in any of the references to modify and combine the structures described in the Kenney, Cogan and Kagaya patents, the combination of the references asserted by the Examiner is not obvious. The mere fact that the references *can* be combined or modified in the manner asserted by the Examiner does not render the resultant combination obvious unless the references also suggest the desirability of such a combination. MPEP § 2143.01. Clearly, none of the references suggest the desirability of such a combination.

It follows that neither Kenney, Cogan, Kagaya, nor their combinations suggest or contemplates the semiconductor body defined in claim 1, and claim 1 is patentably distinct and unobvious over the references.

Claim 2 depends from claim 1 and further defines and limits the invention set out in the independent claim as well as calls for additional limitations. Claim 2 is therefore likewise patentably distinguishable over the references.

Accordingly, the withdrawal of the rejection of claims 1 and 2 under 35 U.S.C. § 103 is respectfully requested.

New claims 21-26 depend from claim 1 and are patentably distinguishable over the cited art at least for the

same reasons. New claims 21 and 22 include limitations previously called for in claim 2. Support for new claims 23-26 is shown in Fig. 10 and described on page 15, line 4 to page 17, line 10 of the specification.

New claim 27 is directed to an isolation structure formed in a semiconductor body and includes limitations similar to those called for in claim 1. Therefore, new claim 27 is distinguishable over the cited references at least for the same reasons. Claims 28-33 depend from claim 27 and are similarly distinguishable over the references. Support for these claims is found as described above with reference to claims 21-26.

As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited.

As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that the Examiner telephone Applicants' attorney at (908) 654-5000 in order to overcome any additional objections which the Examiner might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

By _____

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